

REMARKS

In the Office Action dated October 25, 2005, claims 1-5 and 11-15 were rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 6,492,922, by New (hereinafter New). Claims 6-8 and 16-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over New in view of US Patent Application 2003/0090339, by Xu (hereinafter Xu). In this Amendment, claims 4 and 14 have been canceled and claims 23 and 24 have been added. Accordingly, claims 1-3, 5-13, 15-20, and 23-24 will be pending after entry of this Amendment.

I. Rejection of the Claims Under 35 U.S.C. § 102(b)

In the Office Action, claims 1-5 and 11-15 were rejected under 35 U.S.C. § 102(b) as being anticipated by New. Applicants have amended claim 1 and as the rejection may be applied to amended claim 1, respectfully traverse. Amended claim 1 recites a circuit comprising:

at least one delay element for receiving an input signal and for generating a time delay in said signal to produce a time-delayed signal;
calibration circuit, coupled to said delay element, for calibrating said delay element so as to match said time delay to a predetermined time period, said calibration circuit comprising a control loop for receiving an output signal from said delay element and a reference signal and for generating a phase adjustment based on a phase difference between said output and reference signals; and
multiplier-summing circuit, coupled to said delay element, for multiplying at least one signal output from said delay element to produce at least one multiplied signal and for summing at least one multiplied signal to generate an equalized signal.

Applicants submit that New does not disclose, teach, or even suggest each recited feature of claim 1. For example, New does not disclose, teach, or even suggest a calibration circuit comprising a control loop for receiving an output signal from a

delay element and a reference signal and for generating a phase adjustment based on a phase difference between said output and reference signals, where the delay element is coupled to a multiplier-summing circuit for multiplying a signal output from the delay element and for summing the multiplied signal to generate an equalized signal, as required in claim 1.

In New, the delay elements 106 coupled to the operational amplifier 108 (used for summing weighted signals from the delay elements 106) do not send an output signal to control circuit 112 for phase comparison to a reference signal. Rather, the control circuit 112 receives an output signal from different delay elements 110 that are not coupled to a multiplier-summing circuit for multiplying and summing signals. *See* Figure 2 and column 3, line 34 to column 4, line 24 of New. In other words, New discloses a delay element 106 coupled to an operational amplifier 108 for summing weighted signals and a different delay element that sends an output signal to a control circuit 112. New, however, does not disclose a delay element that is both coupled to the operational amplifier 108 for summing weighted signals and that sends an output signal to the control circuit 112.

As such, New does not disclose a control loop that receives an output signal from a delay element where the same delay element is coupled to a multiplier-summing circuit for multiplying and summing signals from the delay element, as required in claim 1. For the above reasons, Applicants submit that claim 1 is in allowable form. Claims 2-5 are dependent upon claim 1 and allowable for at least the same reasons as claim 1.

Independent claim 11 is a method claim that has been amended to include limitations similar to amended claim 1. Accordingly, claim 11 is in allowable form for the same reasons as stated above for claim 1. Claims 12-15 are dependent upon claim 11 and allowable for at least the same reasons as claim 11.

II. Rejection of the Claims Under 35 U.S.C. § 103(a)

In the Office Action, claims 6-8 and 16-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over New in view of Xu. Claims 6-8 are dependent upon claim 1 and allowable for at least the same reasons as claim 1. Claims 16-18 are dependent upon claim 11 and allowable for at least the same reasons as claim 11.

III. New Claims 23 and 24

New claim 23 is dependent upon claim 1 and allowable for at least the same reasons as claim 1. New independent claim 24 recites a circuit comprising:

at least one delay element for receiving a signal and for generating a time delay in said signal, said delay element comprising a transmission line and a means for adjusting capacitance for said transmission line for calibrating said delay element;

calibration circuit, coupled to said delay element, for calibrating said delay element so as to match said time delay to a predetermined time period; and

multiplier-summing circuit, coupled to said delay element, for multiplying at least one signal output from said delay element and for summing at least one multiplied signal to generate an equalized signal.

[Emphasis added.]

Applicants submit that neither New nor Xu, alone or in combination, disclose, teach, or even suggest each recited feature of new claim 24. In regards to claim 6, the Examiner stated that Figure 2 of Xu discloses a delay element having a transmission line (inductor L) and an adjustable capacitance means such that an accurate delay time is provided. Figure 2 of Xu, however, shows a graph of the output spectrum from a

typical fourth order modulator. Also, Xu relates to a bandpass sigma-delta modulator and does not discuss delay elements anywhere, let alone delay elements having a transmission line (inductor L) and an adjustable capacitance means. As such, Applicants submit that claim 24 is in allowable form.

CONCLUSION

Based on the foregoing remarks, Applicants believe that the application is in condition for allowance. If the Examiner has any questions regarding the case, the Examiner is invited to contact Applicants' undersigned representative at the number given below.

Respectfully submitted,

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